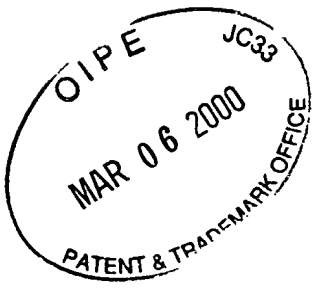

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jeffrey S. Mailloux et al.

Title: ASYNCHRONOUSLY-ACCESSIBLE MEMORY DEVICE WITH MODE SELECTION CIRCUITRY FOR BURST OR PIPELINED OPERATION

Docket No.: 303.623US4
Filed: December 3, 1997
Examiner: Hong Kim

Serial No.: 08/984,563
Due Date: February 29, 2000
Group Art Unit: 2751

Assistant Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Amendment and Response (5 Pages).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described above, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on this 29th day of February, 2000.

By: Daniel J Polglaze

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S/N 08/984,563 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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AMENDMENT AND RESPONSE

Assistant Commissioner for Patents
Washington, D.C. 20231

Applicant has reviewed the Office Action mailed on November 30, 1999. Please amend the above-identified patent application as follows.

IN THE CLAIMS

Please amend the claims as follows:

60. (Amended) The method of claim 59, and further comprising:
switching between [a] the burst mode of operation and [a] the pipelined mode of operation.

61. (Amended) The method of claim 59, and further comprising:
switching between [a] the read operation and [a] the write operation.

65. (Amended) A method of operating a memory circuit, comprising:
receiving a mode select signal;
receiving an initial external address;
selecting a read or a write operation of the memory;
cycling a second enabling signal multiply between active and inactive;
generating an internal address on a cycle of the second enabling signal based on the initial external address;
changing the mode select signal to select a pipeline mode of operation while maintaining [the] a first enabling signal in an active state; and
receiving an external address on each cycle of the second enabling signal.